Vision Chip Architecture Using General-Purpose Processing Elements for 1ms Vision System

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Abstract

This paper describes a vision chip architecture for high-speed vision systems that we propose. The chip has general-purpose processing elements (PEs) in a massively parallel architecture, with each PE directly connected to photo-detectors. Control programs allow various visual processing applications and algorithms to be implemented. A sampling rate of 1ms is enough to realize high-speed visual feedback for robot control. To integrate as many PEs as possible on a single chip a compact design is required, so we aim to create a very simple architecture. The sample design has been implemented into an FPGA chip; a full custom chip has also been designed and has been submitted for fabrication.

1 Introduction

In the field of visual applications like robot vision, traditional vision systems have an I/O bottleneck problem due to scanning and transmitting a large amount of image data, and the sampling rate is limited to video rates. On the other hand a system using a vision chip in which sensors and parallel PEs are integrated will solve the problem. There has been much research on vision chips but many of them have only limited functions because of VLSI implementation problems.

We have been engaged in the researches of high-speed vision from various points of view including the application, the algorithms and the architecture. We aim to build a high-speed vision system based on a vision chip. The system is called 1ms vision system because its sampling rate is less than 1ms for most applications. We have already constructed a target tracking system using visual feedback as an application [1]. Algorithms for the high-speed vision system have also been designed [2]. The important requirements for the vision chip in this system are the massively parallel structure in which the number of pixels corresponds with that of the PEs, and the general-purpose architecture which is adaptive to various applications and environments. Additionally to integrate such an architecture on a single chip a compact design is required. In this paper we propose a general-purpose vision chip architecture using digital technology and report the results of the design and the evaluation.

2 Related research

In the past research and development of vision chips was performed in many research laboratories but they were mostly for specific purposes using analog circuits like a resister network. To realize versatile processing that is adaptive to various and changing environments, it is effective to introduce some form of general-purpose processing element using digital technology and make the vision chip programmable. Ishikawa *et al*. developed an architecture of such a PE and integrated 8 PEs in a gate-array chip (SPE-8) [3]. They also developed a scaled-up model of the vision chip, known as SPE-4k, using 512 LSIs and some discrete components which had 64×64 PEs, photo-detectors, and LEDs. Various applications and algorithms were demonstrated.

Other research on an image processor with digital PEs and photo detectors was done at Linköping University, Sweden [4]. Also at ETCA, France, where the programmable artificial retina was developed [5].
These vision chips using digital PEs require large area and the chips mostly lack generality and usability.

3 S^3PE architecture

To integrate more general-purpose PEs and to make a practical vision chip which can be used for real systems, we have developed a new and much simpler architecture called S^3PE (Simple and Smart Sensory Processing Elements) . We introduce details of the architecture below.

3.1 Structure of the whole chip

The block diagram of the whole chip is shown in Fig.1. Each PE is directly connected to a photo-detector, an output circuit, and its four neighboring PEs. The input

image signals are A/D-converted and transmitted in parallel to all PEs. The instruction codes from the external pins are transmitted to all the PEs and processed simultaneously (SIMD type processing). The resulting data are transmitted to the output circuit and the feature quantities are extracted and transmitted to the external pins.

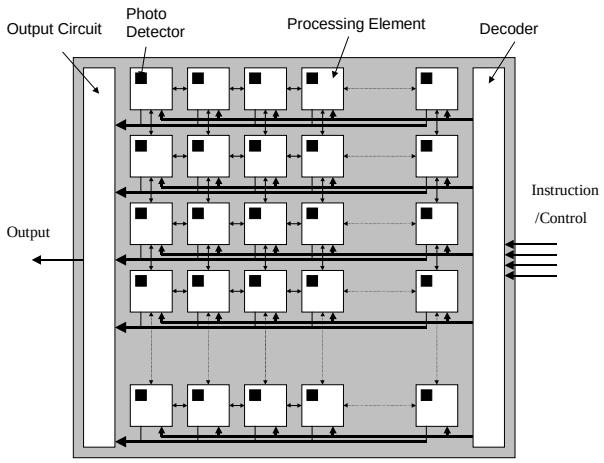

Fig.1 Structure of the whole chip

3.2 Structure of the PE

The block diagram of the PE is shown in Fig.2. Each PE consists of an ALU, local memory and three registers. The ALU takes charge of the calculation and the memory data recording and I/O. Two registers, called A register and B register, read data from the memory and the ALU performs an operation on the data. Then the result is once fetched by the Z register and is written into the memory again. This process is defined as a single cycle and by performing several cycles you can process various kinds of algorithms.

The block diagram of the ALU is shown in Fig.3. The ALU can process one of 10 logical and 8 arithmetic operations at one time. They are all binary operations and multi-bits operations are processed by repeating single operations serially.

The local memory has 5-bit address space and consists of a 24-bit RAM, and an 8-bit memory-mapped I/O connected to a sensor, an output circuit, four-neighboring PEs and ground. Each bit can be randomly accessed. The address map is shown in Table1.

The function of the ALU and the size of the memory are proved to be enough for most early visual processing algorithms which are often used in visual applications.

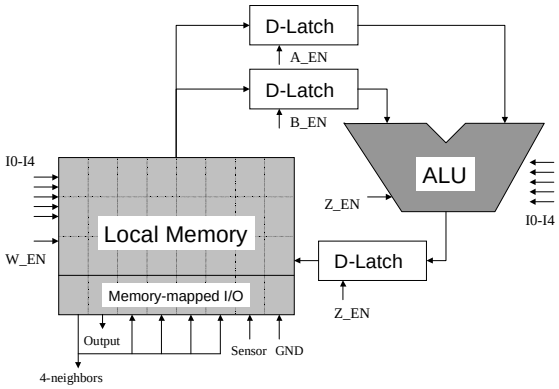

Fig.2 Block diagram of the PE

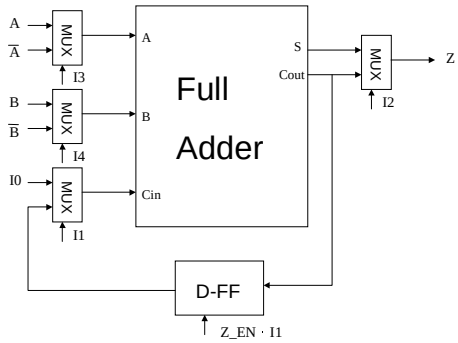

Fig.3 Block diagram of the ALU

Table1 Address map of the local memory

Address	Function
0-23	Random access memory
24	Output to 4 neighbors
25	Output to external
26	Input from up
27	Input from down
28	Input from left
29	Input from right
30	Input from sensor
31	Zero

3.3 Instru

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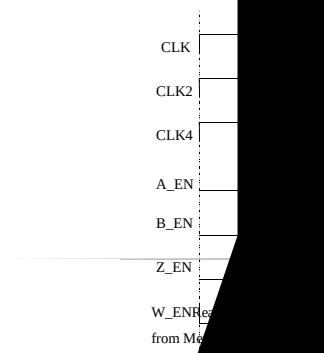

ns/cycle.

We are now developing a vision chip based on the S^3PE architecture. The goal is to make a full custom design with more than 64×64 PEs and photo detectors integrated on a single chip. As steps towards this goal, some sample designs were made.

First, we developed the test chip in the S^3PE architecture using the FPGA technology from Actel Corporation. The chip has 4×4 PEs and some global circuits including an internal clock generator and instruction controller. We also developed a test board for the chip which downloads programs from the host and transmits them to the chip at high speed. In this system the chip works at 154 ns/cycle.

Full-custom prototype designs have been developed and submitted to CMP in France for fabrication. The specification of the most recent version is shown in Table4. The chip has 8×8 PEs in an area of 4.12mm× 3.70mm using a 0.8μm CMOS DLP/DLM process with each PE directly connected to a photo-detector. The area of each PE is about 290μm×390μm. To creduce the area, an SRAM technology is used in the local memory module of each PE. The number of transistors of the PE in this version is 437 per pixel. The chip will come back soon and will be checked. Fig.5 shows the layout of the chip. Newer versions are now being developed.

Table4 Specification of the prototype chip

Process	CMOS 0.8 μm DLP/DLM
Number of pixels	8 × 8 = 64
Number of transistors (PE)	437 per pixel
Number of transistors (PD)	5 per pixel
Total area size	4.1 × 3.7 mm^2
Pizel (PE+PD) area	290 × 390 μm^2
Photodiode area	20 × 20 μm^2
Clock frequency	> 50 MHz
A/D conversion	CMOS thresholding
Local memory type	6 transistor SRAM
Digital power voltage	V_{DD}=5V
Analog power voltage	V_{DDA}=5V
Package	CLCC 84pin

5 Conclusion

In this paper we propose a high-speed vision system using a vision chip with general-purpose PEs. We introduce the architecture of the vision chip for the system. Algorithms and applications for the system were developed. As a result of simplifying the structure the vision chip in our architecture is very compact and easy to use. The FPGA test chip has been made and the full-custom prototype chip has been designed and submitted for fabrication.

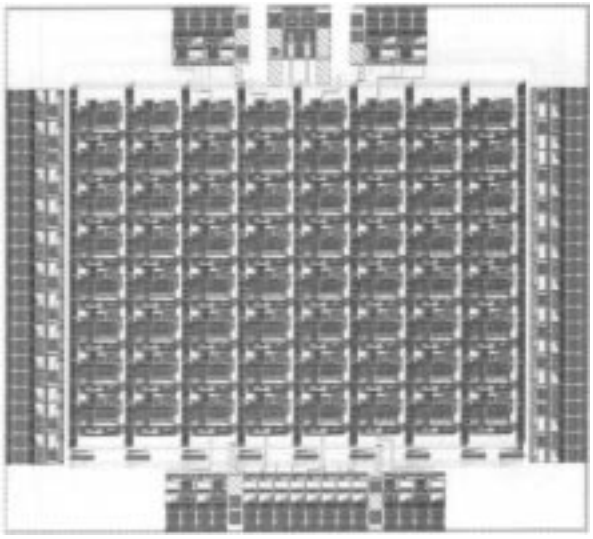

Fig.5 Layout overview of the prototype chip

With the recent progress of VLSI technology, many digital PEs can be integrated on a single chip and a practical programmable vision chip will be realized. In the near future, not only a single chip but also the system including both hardware and software which are co-designed will become more important and the vision chip design considering the whole system will be required.

References

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