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1ms Column Parallel Vision System and It's Application of High Speed Target Tracking

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Abstract

Robot control using a real-time visual feedback has been recently improved (visual servoing.) Conventional vision systems are too slow for these application, because the CCD cameras are restricted to the video frame rate (NTSC 30Hz, PAL 25Hz). To solve this problem, we have developed a 1ms vision system, to provide a far faster frame rate than that of the conventional systems.

Our 1ms vision system has a 128×128 PD array and an all parallel processor array connect to each other in a column parallel architecture, so that the bottleneck of an image transfer has been solved. 1ms visual feedback has been realized in this system, in which the image feature value is extracted in 1ms cycle-time for visual servoing. We have also developed a high speed Active Vision System (AVS)-II, which makes a gaze of vision system to move at high speed.

In this paper, we will provide a detail discussion on our 1ms vision system and its performance through some experiments.

1 Introduction

It is effective to use visual feedback information for systems such as for controlling robots or autonomous land vehicles. In recent years, the study, which realizes visual feedback by a real-time closed loop is popular, these technique is called visual servoing.

But, most of the conventional vision systems are using CCD cameras for image sensing. The transmission speed of an image on these systems has been limited to video rate (NTSC 30Hz, PAL 25Hz). Therefore, the operation speed of the system has been limited to that of the video rate, even if fast image processing had been carried out. This limitation causes a serious problem when realizing a visual servo control, because it is generally accepted that a servo rate around 1kHz is needed for robot control. Essentially the sampling rate of conventional vision systems is too slow compared to the robot dynamics.

The origin of such a problem lies in the bottleneck of the image transmission. That is to say, high-speed frame rate is difficult to realize using the transmittion of the image information, which consists of a lot of pixel datas, through the small number of lines.

On the other hand, Ishikawa et al. have developed a vision chip, and proposed its architecture of S^3PE (Simple and Smart Sensory Processing Elements) in which all photo-detectors (PDs) are directly connected to the parallel processing elements (PEs) [1, 2]. These PEs are integrated into one chip so that the bottleneck of the image transmission does not occur and therefor realization of high speed vision systems becomes possible which can provide far faster frame rate than conventional vision systems.

But in this way, a lot of sensors and processing elements must be integrated into one chip, so that the circuit of the processing elements should be compactly designed. Yet this requirement disagrees with the needs to have an ability to carry out various kinds of image processing completed on the PEs. It is reported that 64×64 pixels are the realistically possible limit with satisfying these competitive requests fabricated by the present semiconductor technology [1].

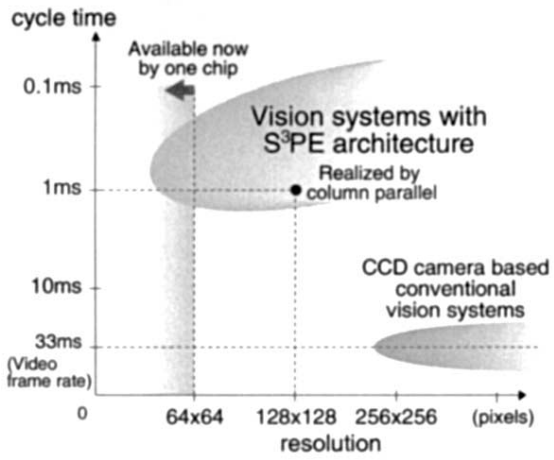


Figure 1 Comparison with conventional image systems

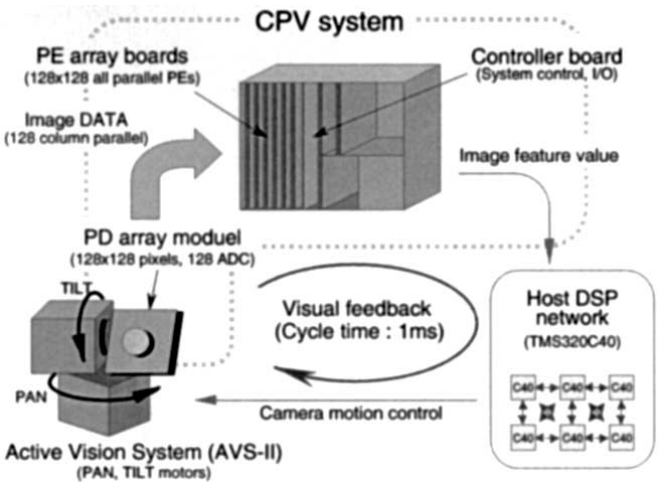


Figure 2 Overview of 1ms vision system

2 Column Parallel Approach

In contrast to these approaches, the system that we developed uses a column type parallel image transfer

tems [3, 4, 5]. Furthermore, we proposed a novel approach in high-speed image processing and developed various kinds of algorithms utilizing the characteristic of the high frame rate of the vision system [6, 7]. These papers discuss that the high-speed vision sys-

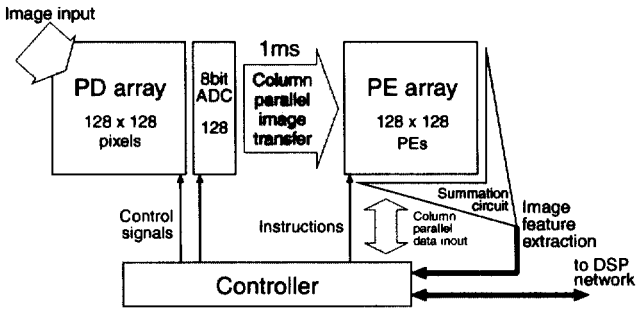


Figure 3 Column Parallel Vision(CPV) system

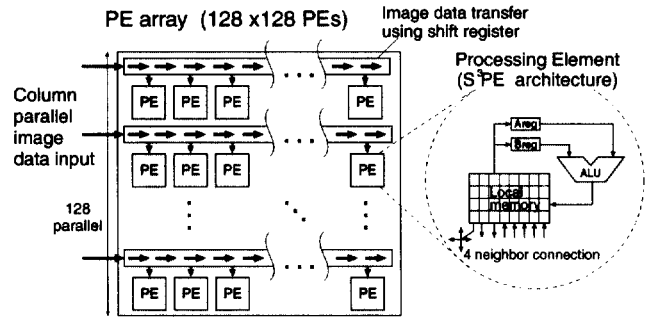


Figure 4 S^3PE architecture with column parallel data transfer

motion control.
An overview of the whole system is shown in Fig. 2.

3.1 Column Parallel Vision (CPV) System with 128×128 Pixels

In the CPV system, various image processing algorithms applied after the image acquisition which was followed by the extraction of the image feature value as the output to the DSP (Digital Signal Processor) element. This information is used for the visual feedback control.
Inside the CPV system, there are three modules, namely a PD array, a PE array and a controller. The block diagram of the CPV system is shown in Fig. 3. At the following paragraph, details in each systems are described.

3.1.1 PD Array

The PD array consists of photo-detectors and an AD converter array which are integrated into one chip. The resolution of the PD array is 128×128 pixel. AD converter array is in 128 lines column parallel and have an 8-bits gray scale resolution. The output image data from a selected row in PD array is transmitted to the PE array in 128 lines column parallel. As a result, all the pixel data of each frame can be read in around 1 ms.

3.1.2 PE Array

The image processing part consists of 128×128 parallel PEs array that realizes a totally parallel processing in each pixel of the image. The inner structure of the PEs is based on the S^3PE architecture [2], which adopts a SIMD type program control, 4-neighbor connection, a bit serial ALU, 24-bits local memory and memory mapped I/Os. These all are to satisfy the needs of compactness and functionality. The controller sends the instructions for the PEs. Full descriptions of the controller are written in the next paragraph.
The datas of pixels from PDs are transferred to the corresponding PEs by using shift registers implemented in the CPV system. Using this interface, the sensor datas are forwarded one bye one from selected column of the PD array, and are taken in the PEs with corresponding column.
For the implementation of this massively parallel PE array, 128 chips (XILINX XC4044XL) of FPGA (Field Programmable Gate Array) are used. Every chip has 16×8 PEs and all the chips are loaded on eight sheets of circuit boards. 1 instruction of the system is executed within 330ns at present.
The figure 4 shows the architecture of S^3PE with column parallel data transfer used in the PE array.

3.1.3 Controller

In general, when constructing a parallel processing system, the role of controller is important, which regulates the operation of the whole system and carries an interface with outer system without the bottleneck.
An architecture of the controller is shown in Fig.5.
Corresponding to the purpose of the CPV system given at the beginning of this section, the functions realized in this controller are described as follows.

- Extracting and calculating image feature values :
  Extracting and calculating image feature value as a result of processing in the PE array. An exclusive circuit makes it possible to summarize all outputs of PEs without any delay.
- The interface of data in/out with the PE array :
  Carrying out 128-line parallel data input/output with the PE array.

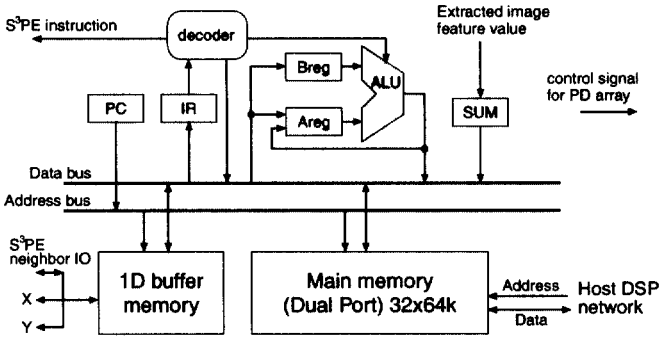


Figure 5 Architecture of Controller

- The SIMD control of the S^{3}PE :
  Sending instructions to the PE array and regulating SIMD control.
- The control of the system by the user program :
  Being all operation of the system controlled by the user program which is downloaded to the main memory.
- The interface with the outer system :
  Caring out data input/output without the bottleneck with host DSP system using the sharing memory method.
- Managing the synchronization of the total system :
  Managing the synchronization of all modules in the CPV system.

An implementation of the controller is also realized by FPGA. It uses two chips (XILINX XC4044XL) loaded on one board.
As a result, the CPV system satisfies the goal of the cycle time of 1ms, because a series of processing and a flow of information for the visual feedback control are ideally implemented without the bottleneck.

3.2 Active Vision System (AVS)-II

The AVS-II is an actuator part of the 1ms vision system to make a gaze move at high speed. The PD array is loaded on the mobile platform which has two degrees of freedom; pan and tilt; and each axes have the Σ-II AC servo motor (100W) made by Yaskawa electric corporation. The motors are used by direct drive and without any gears which allows it to remove the disturbance of the effects of the friction. High power and compact size are realized together with the fast response time compared to the previous version of our active vision system [3, 6].

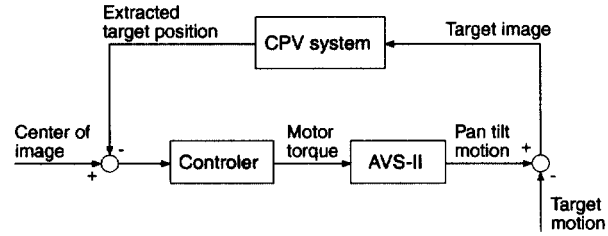


Figure 6 Block diagram of AVS-II control

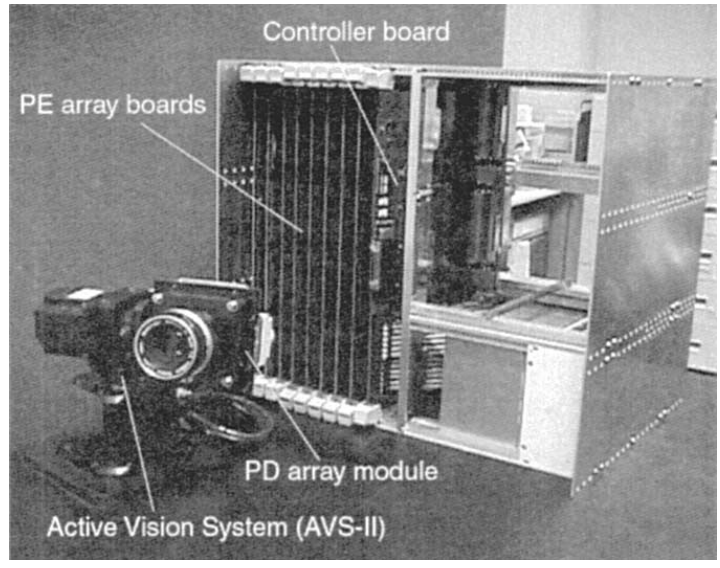


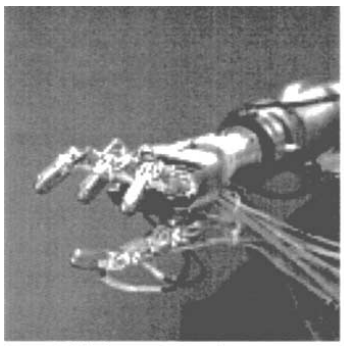
Figure 7 CPV system with AVS-II

The control of the motion are carried out in the host DSP network which used parallel processing DSPs (TMS320C40 by TI). Using the DSP network enables 1ms cycle time without bottleneck dispersing load of the processing and I/Os [5].
The block diagram of the control of the AVS-II is shown in Fig.6. A real-time visual servo control by the method of torque control is constructed.
The photograph of the CPV system and the AVS-II is shown in Fig.7.

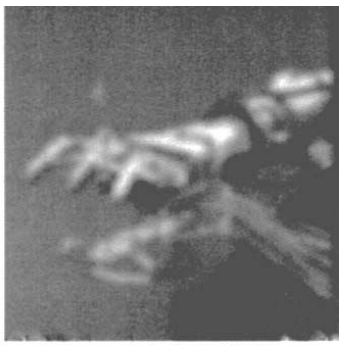
4 Experimental results

4.1 High Speed Image Processing

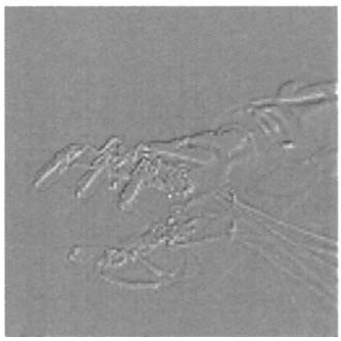
At first, several kinds of generally used image processing had been carried out to confirm the performance of the CPV system.
In the experiments, 8-bits digitized images are continuously obtained at PD array. Image processing is applied at every frame cycle carried out by parallel



8bit Input raw image



7times 4-Blured image



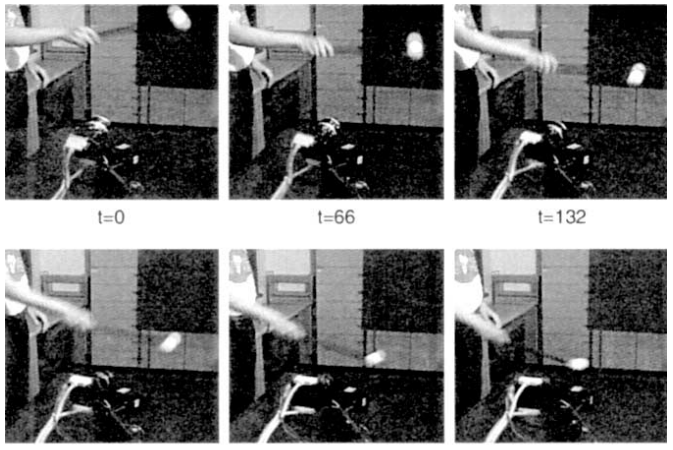


Figure 9 Photo strip of target tracking

processing contents	steps	time
3-bits data input	3	1.0 μs
filtering	41	13.6 μs
self windowing	6	2.0 μs